

**Claim Amendments**

Please amend claims 1 and 12 as follows:

Please cancel claims 6 and 17 as follows:

**Claims as Amended**

1. (currently amended) A method for forming a single transistor planar RAM memory cell with improved charge retention comprising the steps of:

providing a silicon substrate comprising an STI structure and an overlying dielectric gate layer;

depositing a polysilicon layer;

forming a pass transistor structure adjacent a storage capacitor structure separated by a predetermined distance;

carrying out a first ion implantation process to form first and second doped regions adjacent either side of the pass transistor structure, the first doped region defined by the predetermined distance;

depositing a spacer dielectric layer;

etching back the spacer dielectric layer to leave an unetched spacer dielectric layer portion overlying the first doped region while forming a sidewall spacer of a predetermined width overlying a first portion of the second doped region;

wherein the predetermined distance is less than about twice the predetermined width; and,

carrying out a second ion implantation process to form a relatively higher dopant concentration in a second portion of the second doped region.

2. (original) The method of claim 1, further comprising the step of forming self aligned silicide regions over the second portion, the pass transistor structure and the storage capacitor structure.

3. (original) The method of claim 1, wherein the dielectric gate layer is selected from the group consisting of SiO<sub>2</sub>, nitrided SiO<sub>2</sub>, and oxide/nitride.

4. (original) The method of claim 1, wherein the dielectric gate layer comprises material selected from the group consisting of Ta<sub>2</sub>O<sub>5</sub>, TiO<sub>2</sub>, HfO<sub>2</sub>, Y<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>5</sub>, ZrO<sub>2</sub>, BST, and PZT.

5. (original) The method of claim 1, wherein the storage capacitor structure is formed at least partially overlying the STI structure.

6. cancelled

7. (original) The method of claim 1, wherein the spacer dielectric layer thickness is about greater than about half of the predetermined distance.

8. (original) The method of claim 1, wherein the pass transistor structure and the storage capacitor structure comprise a memory cell formed over an N doped well region of a P doped silicon substrate.

9. (original) The method of claim 1, wherein the first and second doped regions respectively comprise P- and P+ doped regions.

10. (original) The method of claim 1, wherein the first doped region is doped to a level of between about  $10^{12}$  and  $10^{14}$  dopant atoms/cm<sup>2</sup> and the second doped region comprises a relatively higher doped region of greater than about  $10^{15}$  dopant atoms/cm<sup>2</sup>.

11. (original) The method of claim 1, wherein the spacer dielectric layer comprises one or more layers selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

12. (currently amended) A method for forming a single transistor planar RAM memory cell with improved charge retention comprising the steps of:

providing a silicon substrate comprising an STI structure and an overlying dielectric gate layer;

depositing a polysilicon layer;

forming a pass transistor structure adjacent a storage capacitor structure separated by a predetermined distance for forming a first doped region;

carrying out a first ion implantation process to form the first doped region and a second doped region adjacent the pass transistor structure;

blanket depositing a spacer dielectric layer having a thickness about greater than the predetermined distance;

etching back the spacer dielectric layer to leave an unetched spacer dielectric layer portion overlying the first doped region while forming a sidewall spacer overlying a first portion of the second doped region;

wherein the predetermined distance is less than about twice the sidewall spacer width; and,

carrying out a second ion implantation process to form a relatively higher dopant

concentration in a second portion of the second doped region.

13. (original) The method of claim 12, further comprising the step of forming salicide regions over the second portion, the pass transistor structure and the storage capacitor structure.

14. (original) The method of claim 12, wherein the dielectric gate layer is selected from the group consisting of  $\text{SiO}_2$ , nitrided  $\text{SiO}_2$ , and oxide/nitride.

15. (original) The method of claim 12, wherein the dielectric gate layer comprises material selected from the group consisting of  $\text{Ta}_2\text{O}_5$ ,  $\text{TiO}_2$ ,  $\text{HfO}_2$ ,  $\text{Y}_2\text{O}_3$ ,  $\text{La}_2\text{O}_5$ ,  $\text{ZrO}_2$ , BST, and PZT.

16. (original) The method of claim 12, wherein the storage capacitor structure is formed at least partially overlying the STI structure.

17. cancelled

18. (original) The method of claim 12, wherein the pass transistor structure and the

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storage capacitor structure comprise a memory cell formed over an N doped well region of a P doped silicon substrate.

19. (original) The method of claim 12, wherein the first and second doped regions respectively comprise P- and P+ doped regions.

20. (original) The method of claim 12, wherein the first doped region is doped to a level of between about  $10^{12}$  and  $10^{14}$  dopant atoms/cm<sup>2</sup> and the second doped region comprises a relatively higher doped region of greater than about  $10^{15}$  dopant atoms/cm<sup>2</sup>.

21. (original) The method of claim 12, wherein the spacer dielectric layer comprises one or more layers selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

claims 22-32 cancelled